Electronics

1) What should be the value of laplace transform for the time-domain signal equation e-at cos ωt.u(t)?

a. 1 / s + a with ROC σ > - a
b. ω / (s + a) 2 + ω2 with ROC σ > - a
c. s + a / (s + a)2 + ω2 with ROC σ > - a
d. Aω / s2 + ω2 with ROC σ > 0

ANSWER: s + a / (s + a)2 + ω2 with ROC σ > - a

2) According to the time-shifting property of Laplace Transform, shifting the signal in time domain corresponds to the _____

a. Multiplication by e-st0 in the time domain
b. Multiplication by e-st0 in the frequency domain
c. Multiplication by est0 in the time domain
d. Multiplication by est0 in the frequency domain

ANSWER: Multiplication by e-st0 in the frequency domain

3) Which result is generated/ obtained by the addition of a step to a ramp function?

a. Step Function shifted by an amount equal to ramp
b. Ramp Function shifted by an amount equal to step
c. Ramp function of zero slope
d. Step function of zero slope

ANSWER: Ramp Function shifted by an amount equal to step

4) Unilateral Laplace Transform is applicable for the determination of linear constant coefficient differential equations with _____

a. Zero initial condition
b. Non-zero initial condition
c. Zero final condition
d. Non-zero final condition

ANSWER: Non-zero initial condition

5) Two vectors a, b are orthogonal if

a. <a,b> = 0

b. <a,b> = <a,b>
c. <a,b> = 1
d. <a,b> = - <a,b>

ANSWER: <a,b> = 0

6) One dimensional signal is a function of

a. Multiple independent variables
b. Single independent variable
c. Multiple dependent variables
d. Single dependent variable

ANSWER: Single independent variable

7) Superposition of signals in a linear system refers to the

a. Output that is product of all the signals
b. Output that is sum of all the signals
c. Output that is of highest amplitude of all the signals
d. Output that is of largest spectrum of all the signals

ANSWER: Output that is sum of all the signals

8) The scaling of a sequence x[n] by a factor α is given by

a. y[n] = α [x[n]]2
b. y[n] = α x[n2]
c. y[n] = α x[n]
d. y[n] = x[n]x[-n]

ANSWER: y[n] = α x[n]

9) DFT is applied to

a. Infinite sequences
b. Finite discrete sequences
c. Continuous infinite signals
d. Continuous finite sequences

ANSWER: Finite discrete sequences

10) Which among the following EDA tool is available for design simulation?

a. OrCAD
b. ALDEC
c. Simucad
d. VIVElogic

ANSWER: VIVElogic

11) Which among the following functions are performed by MSI category of IC technology?

a. Gates, Op-amps
b. Microprocessor/A/D
c. Filters
d. Memory/DSP

ANSWER: Filters

12) The 'next' statements skip the remaining statement in the _____ iteration of loop and execution starts from first statement of next iteration of loop.

a. Previous
b. Next
c. Current (present)
d. None of the above

ANSWER: Current (present)

13) An Assert is _____ command.

a. Sequential
b. Concurrent
c. Both a and b
d. None of the above

ANSWER: Both a and b

14) Timing analysis is more efficient with synchronous systems whose maximum operating frequency is evaluated by the _____path delay between consecutive flip-flops.

a. shortest
b. average

c. longest
d. unpredictable

ANSWER: longest

15)   Which kind of low-order 16 bits control register is also regarded as 'Machine Status Word' (MSW) in order to make it compatible with i286?

a. CR0
b. CR1
c. CR2
d. CR3

ANSWER: CR0

16)   In the test registers, what do/does the linear address bit hold/s with respect to TLB (Translation Look-aside Buffers)?

a. Physical address
b. Selection between write and lookup of TLB
c. Tag field
d. All of the above

ANSWER: Tag field

17)   For addressing in real mode, which segment plays a significant role in the storage of destination operands during the string operation?

a. Code Segment
b. Data Segment
c. Stack Segment
d. Extra Segment

ANSWER: Extra Segment

18)   In x86 architecture, which type of gate acts as an intermediary between code segments at different privilege levels (PLs)?

a. Call gates
b. Task gates
c. Interrupt gates
d. Trap gates

ANSWER: Call gates

19)   In Pulse Position Modulation, the drawbacks are

a. Synchronization is required between transmitter and receiver
b. Large bandwidth is required as compared to PAM
c. None of the above
d. Both a and b

ANSWER: Both a and b

20)   In PWM signal reception, the Schmitt trigger circuit is used

a. To remove noise
b. To produce ramp signal
c. For synchronization
d. None of the above

ANSWER: To remove noise

21)   In pulse width modulation,

a. Synchronization is not required between transmitter and receiver
b. Amplitude of the carrier pulse is varied
c. Instantaneous power at the transmitter is constant
d. None of the above

ANSWER: Synchronization is not required between transmitter and receiver

22)   In different types of Pulse Width Modulation,

a. Leading edge of the pulse is kept constant
b. Tail edge of the pulse is kept constant
c. Centre of the pulse is kept constant
d. All of the above

ANSWER: All of the above

23)   In Pulse time modulation (PTM),

a. Amplitude of the carrier is constant

b. Position or width of the carrier varies with modulating signal

c. Pulse width modulation and pulse position modulation are the types of PTM

d. All of the above

ANSWER: All of the above

24)   Which among the following units of PLC is adopted to convey the control plan to CPU?

a. Memory

b. Power supply unit

c. I/O interface

d. Programming software

ANSWER: Programming software

25)   Which architectural unit/block of PLC decides the sequence of different operations to be executed by means of instructions written in memory?

a. Memory

b. Programming software

c. I/O interface

d. CPU

ANSWER: CPU

26)   Which among the following is a unique model of a system?

a. Transfer function

b. State variable

c. Both a and b

d. None of the above

Answer Explanation Related Ques

ANSWER: Transfer function

27)   Which among the following is a disadvantage of modern control theory?

a. Implementation of optimal design

b. Transfer function can also be defined for different initial conditions

c. Analysis of all systems take place

d. Necessity of computational work

Answer Explanation Related Ques

ANSWER: Necessity of computational work

28) Match the following value kind attributes with their return elements :

A. Value Type attribute -------------------- 1) Length
B. Value Array attribute ------------------- 2) Information
C. Value Block attribute ------------------- 3) Bounds

a. A- 3, B- 1, C- 2
b. A- 1, B- 2, C- 3
c. A- 2, B- 1, C- 3
d. A- 2, B- 3, C-1

ANSWER: A- 3, B- 1, C- 2

29) Which among the following is not a type of concurrent statement?

a. Simple signal assignment
b. Selected signal assignment
c. Generate statement
d. Direct Instantiation

ANSWER: Direct Instantiation

30) Which type of logic is produced by case statements?

a. Serial logic
b. Parallel logic
c. Priority encoded logic
d. Priority decoded logic
ANSWER: Parallel logic

31) Which among the following does not belong to the category of sequential statements?

a. If statements
b. Process statements
c. Loop statements
d. Node statements

ANSWER: Node statements

32)   Which among the following ROMs exhibit/s the necessity of eliminating the PROM from the circuit?

a. EPROM
b. EEPROM
c. Both a and b
d. None of the above

ANSWER: EPROM

33)   What is the major functioning role of VVR in the multistage AGC amplifier circuit during an increment in the signal level?

a. Variation in control of input signal level
b. Variation in voltage gain of multistage amplifier
c. Variation in current gain of multistage amplifier
d. Variation in control of output signal level

ANSWER: Variation in voltage gain of multistage amplifier

34)   The rectified & filtered signal taken at a high level point in AGC amplifier generates _____.

a. dc voltage proportional to the level of an output signal
b. dc voltage proportional to the level of an input signal
c. ac voltage proportional to the level of output signal
d. ac voltage proportional to the level of an input signal

ANSWER: dc voltage proportional to the level of an output signal

35)   How does the FET operate before the pinch-off region with small value of drain-to-source voltage in accordance to the control of drain-to-source resistance by the bias voltage?

a. As a Voltage Controlled Resistor
b. As a Voltage Dependent Resistor
c. As a Voltage-Variable Resistor
d. All of the above

ANSWER: All of the above

36)   How are the zener diodes placed internally in MOSFETs so as to provide defence from the hazardous consequences of stray voltages?

a. Alternately
b. Opposite to each other
c. Back-to-back
d. All of the above

ANSWER: Back-to-back

37)   FETs are widely applicable in oscilloscopes and voltmeters as an input amplifier as compared to bipolar transistors due to _____.

a. ability of minimizing the loading effect with high input resistance
b. ability of maximizing the loading effect with high input resistance
c. ability of minimizing the loading effect with low input resistance
d. ability of maximizing the loading effect with low input resistance

ANSWER: ability of minimizing the loading effect with high input resistance

38)   Which mode is produced by a positive swing in gate-to-source voltage by input ac signal with the maximum voltage drop across load resistor in DE-MOSFET amplifier circuit?

a. Depletion mode with decrease in drain current
b. Enhancement mode with decrease in drain current
c. Depletion mode with an increase in drain current
d. Enhancement mode with an increase in drain current

ANSWER: Enhancement mode with an increase in drain current

39)   How is the layer of P-substrate, that intimate the provision of channel for electrons by touching substrate to metal -oxide film with the semantic behaviour of N-channel, can be referred as?

a. N-type Inversion layer
b. P-type Inversion layer
c. Both a & b
d. None of the above

ANSWER: N-type Inversion layer

40)   The input current of JFET and MOSFET are basically the leakage currents of _____ & _____ respectively

a. forward-biased PN junction & capacitor
b. reversed-biased PN junction & capacitor
c. forward-biased PN junction & inductor
d. reversed-biased PN junction & inductor

ANSWER: reversed-biased PN junction & capacitor